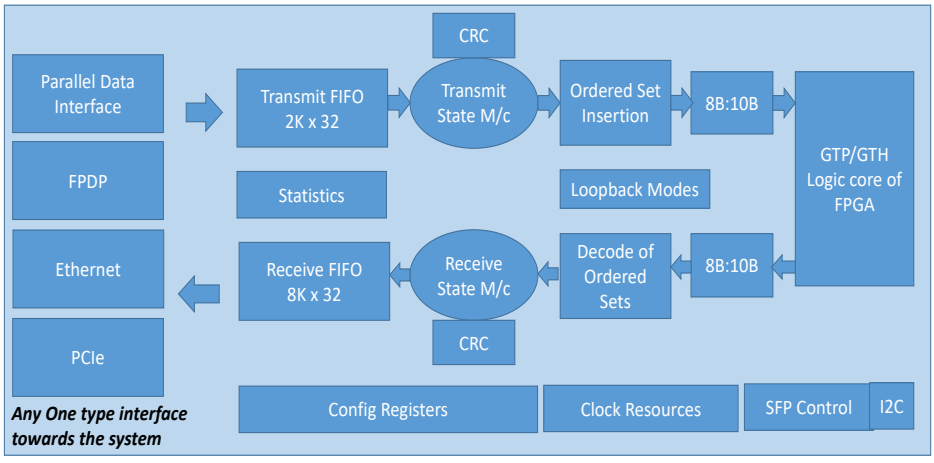
IP Core - sFPDP

Serial Front Panel Data Port (Serial FPDP) Cores for FPGAs/ASICs

Key Features

- ANSI-VITA 17.1- 2003 [and ANSI-VITA 17.1-2015]
- Designed for FPGA based targets.
- Low-Latency serial data transmission protocol.
- It also supports buffer control, different framing formats and low speed control transfer.
- Logic Core is written in Verilog.



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IP Core - sFPDP

Specifications

Link Bandwidth

- 1.0625Gbps
- 2.125Gbps
- 2.5Gbps
- 10Gbps

Framing Formats

- Unframed Data
- Single Framed Data
- Fixed Size Repeating Data
- Dynamic Size Repeating Data.

System Configuration

- Basic or Unidirectional Data Transfer
- Bidirectional with Flow Control
- Bidirectional w/o Flow Control

Serial Transmission

- 8B/10B Line Coding
- Ordered sets support
- Max fiber frame size is 518x4 bytes
- Optional CRC

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Description

Vibhatsu's SFPDP Logic core meets ANSI-VITA 17.1- 2003 [and ANSI-VITA 17.1-2015], designed for FPGA based targets. It comes with a simulation model and relevant porting documents.

Serial Front Panel Data Port [SFPDP] is a High-Speed, Low-Latency serial data transmission protocol, used as an extension of the standard ANSI-VITA 17.0 also called as FPDP. Apart from high speeds like 1.0625 Gbps to upto 10Gbps, it also supports buffer control, different framing formats and low speed control transfer.

Vibhatsu's logic core uses GTP port of the FPGA's for line side implementation, while system side can be a parallel bus, or FPDP or Ethernet or PCIe. Configuration registers can be accessed through the system side interfaces.

Logic core is written with Verilog and Simulation test bench uses Verilog and scripting languages.

Synthesis and Simulation Support

Supported to FPGA IDEs like ISE, Vivado, Libero ,Quartous
Synthesis: Exemplar, Synplicity®, Design Compiler®,FPGA Compiler™, Simplify premier
Simulation: Questasim, VCS

Supported FPGA Families

Xilinx and Intel FPGA's.

Deliverables

The IP-Core is delivered in form of Netlist or Source Code(Verilog).

User Manual.