JESD204C Logic Core

Applications

- High Speed Data Acquisition Systems
- Radar Systems
- Software Defined Radio

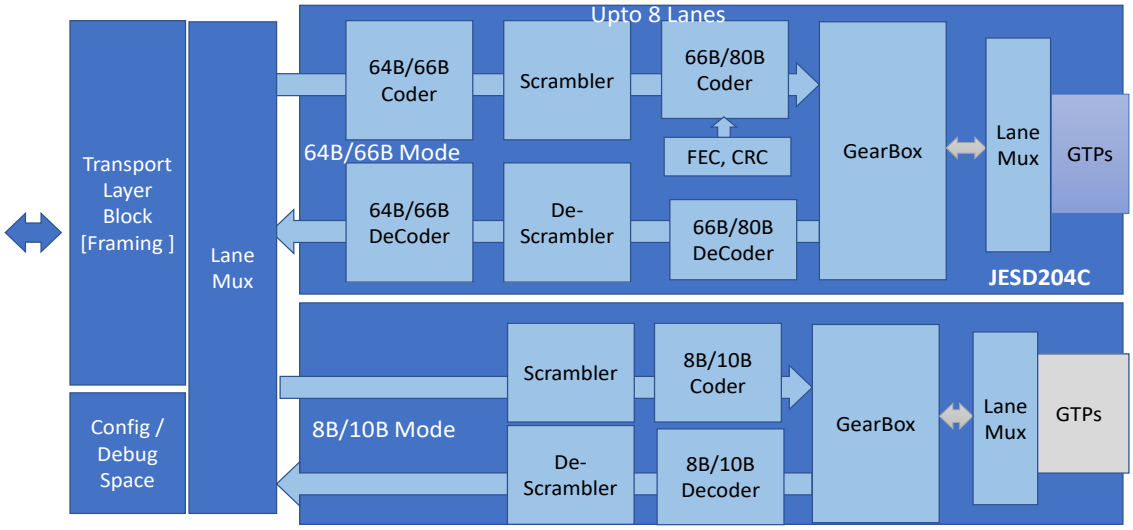
Supported FPGA Families

- Xilinx and Intel FPGA's.

Deliverables

- The IP-Core is delivered in form of Netlist or Source Code(Verilog).
- User Manual.

Block Diagram



Overview:

The JESD204C FPGA IP core is a high-speed multi-lane data interface for ADCs and DACs. It is fully compliant to JEDEC standard JESD204C.1 [Dec2021]. It supports per lane speed of 16Gbps with 64b66b encoding, also supports 8B/10B encoding [due to line coding overhead with 8B/10B, actual line rate is 25% lower]. Supports a total of 8 lanes [can be increased based on overall speed], system side interface supports up to 512 bit wide data bus.

Key Features:

- Designed to JEDEC JESD204C.1 specification
- Line rates from 1 Gb/s to 16 Gb/s [limited by used FPGA]
  - Per lane bus width is 64 bit wide. System side bus is based on number of channels [to save logic]. Max width is 512 bits.
- Supports 1-8 lanes
- Generates initial lane alignment sequence
- Performs the alignment character generation
- Sources link configuration data with user selected parameter values during initial lane synchronization sequence
- 8b-10b, 64b-66b, 64b-80b encoding/decoding supported
- Selectable Scrambling or Bypass. Same for the use of CRC12, CRC3 and FEC
- Verilog-based design
- Optional data mapping and de-mapping
- Supports Subclasses 0, 1 and 2
- Includes PRBS31 data generation and testing [GTP loopback]
- Overall thru delay for data is 9 clocks approx. [doesn't include GTP delay] – uses 1K deep FIFO at gearbox interface for clock, 1K deep FIFO at system side interface for data holding
- Includes debug sections [counters, error monitors, status info etc] to help the tests